

KOREAN PATENT ABSTRACTS

(11)Publication number: 1020010054164 A
(43)Date of publication of application: 02.07.2001

(21)Application number: 1019990054835
(22)Date of filing: 03.12.1999
(51)Int. Cl: H01L 21/762

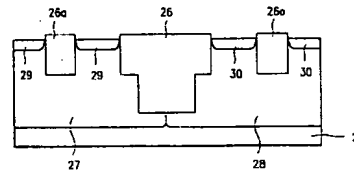
(71)Applicant: HYNIX SEMICONDUCTOR INC.
(72)Inventor: CHO, SEOK WON

(54) FORMING METHOD OF DUAL STI

(57) Abstract:

PURPOSE: A forming method of dual STI(Silicon Trench Isolation) is provided to reduce cell size by minimizing wall space.

CONSTITUTION: The first and the second insulating layers are built on a semiconductor substrate(21). To define an active surface, the second insulating layer is etched selectively using an active mask, and the second isolation pattern is formed. The second isolation layer is used as a mask, the first trench and the second trench are made by etching the first insulation layer and the substrate(21). The third insulating layer is doped on the whole the substrate. In the sidewall of the first trench, a sidewall spacer is constructed, and the third insulating layer fills in the second trench. The fourth insulating layer(26) is deposited and flattened. Through the step, a T-shape of wall STI(Silicon Trench Isolation)(26) and an isolation region(26a) are produced. The active surface is defined by removing the second and the first insulating layers. Inserting p-conductive ions and n-conductive ions, a p-wall region(27) and an n-wall region(28) are formed, respectively. An impurity diffusion region(29) is made with injecting n-conductive impurity ions into the p-wall region(27). As the same way, the other impurity diffusion region(30) is built with inserting p-conductive impurity ions into the n-wall region(28).



COPYRIGHT 2001 KIPO

Legal Status

Date of request for an examination (19991203)
Notification date of refusal decision (20020417)
Final disposal of an application (rejection)
Date of final disposal of an application (20020417)